IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael T. Moore		
Assignee:	Cypress Semiconductor Corporation		
Title:	CONFIGURABLE DEDICATED LOGIC IN CPLDs		
Serial No.:	09/804,523	Filed:	March 12, 2001
Examiner:	Tran, A.	Art Unit:	2819
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Commissioner for Patents
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DECLARATION OF MICHAEL T. MOORE PURSUANT TO 37 C.F.R. § 1.132

I, Michael T. Moore hereby declare as follows:

1. I am presently employed as a Patent Agent by Cypress Semiconductor Corporation.

2 I have been employed by Cypress since August 1998 in various capacities including an Application Engineer and a Senior Application Engineer.

3. A copy of my curriculum vitae is attached to this declaration.

4. I have reviewed both (i) the claims of the present invention and (ii) U.S. Patent No. 5,874,834 to New.

5. I understand that in one embodiment the present invention concerns:

An apparatus comprising:

one or more logic circuits configured to provide logical operation, wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

6. I understand that in another embodiment the present invention concerns:

An apparatus comprising:

means for receiving one or more input signals; and

means for performing logical operation on said input signals using (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

7. I understand that in another embodiment the present invention concerns:

A method for computing in a programmable logic device (PLD) comprising the steps of:

(A) receiving one or more input signals;

(B) performing logical operation on said one or more input signals with (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within said programmable logic device, wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

8. U.S. Patent No. 5,874,834 to New does not disclose and would not suggest a non-programmable hard wired block having no programmable elements, as presently claimed.

9. Based upon my experience and work in the field of semiconductors, a Sea-of-Gates (SOG) gate array as contained in New would not be considered a non-programmable block or logic element.

10. Specifically, a SOG gate array is known in the art as a type of mask-programmable logic array (See "98. Array Circuit Types", Electronics Engineers' Handbook, Third Ed., McGraw-Hill, Inc., 1989, page 8-102-103; attached as Exhibit A).

11. A SOG gate array contains a number of uncommitted gates which can be interconnected (i.e., programmed) by application of one or more metal layers to form a custom-circuit logic function (See the definition of Gate Array on page 8-103 in Exhibit A).

12. Even after a gate array has been programmed, a number of the gates (i.e., programmable elements) can remain uncommitted (i.e., programmable).

13. An SOG gate array can be reprogrammed by adding additional mask layers or etching the previously formed metal layers.

14. The terms dedicated logic, hard wired block, and non-programmable logic element would not be understood in the art to refer to a programmable gate array logic.

15 I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or patents issued therefrom.

Michael T Moore Date: 7/18/03

Michael T. Moore